**Mapping CPU memory address to topological memory address**

32 16 9 7 5 2 0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Row | Column (High Order) | Bank Group | Bank | Column  (Low Order) | Bytes |

* Byte select are LSB (because DIMM delivers 8 bytes in parallel)
* To take advantage of burst, least significant 3 bits of column are used next
* To avoid delay from reads to same bank group, 2 bits for bank group used next
* Then 2 bits of bank
* The remaining (7) column bits come next
* The (16) row bits come next